Japanese Unexamined Patent Publication No. Hei 07-161852

[Claim(s)]

[Claim 1] The memory cell array by which the memory cell which carried out the laminating of a charge accumulation layer and the control gate, was constituted on the semi-conductor layer, and enabled electric rewriting has been arranged in the shape of a matrix, A threshold detection means to charge the bit line connected to said memory cell through this memory cell, said threshold detection means -- the non-volatile semiconductor memory characterized by what it has the sense amplifier which senses the potential of the charged bit line, and the bit line potential by said threshold detection means is controlled for so that it is determined by the threshold of said memory cell.

[Claim 2] The memory cell array by which the memory cell which enabled electric rewriting which carries out the laminating of a charge accumulation layer and the control gate, is constituted on a semi-conductor layer, and carries out the multiple-value storage of two or more three or more data with a threshold has been arranged in the shape of a matrix, A threshold detection means to charge the bit line connected to said memory cell through this memory cell, and to output the multiple-value data of a memory cell to a bit line as potential of multiple-value level, said threshold detection means -- the non-volatile semiconductor memory characterized by coming to provide the sense amplifier which senses the bit line potential of the charged multiple-value level.

[Claim 3] The every series connection of two or more said memory cells is carried out, and they form the NAND cellular structure. The end of a NAND cel is connected to a bit line through the 1st selector gate, and the other end of a NAND cel is connected to a source line through the 2nd selector gate. Said threshold detection means A source line electrical potential difference is made to transmit to a bit line through a NAND cel, and a bit line is charged. The selector-gate electrical potential difference of non-choosing control gate voltage and the 1st, and 2 The non-volatile semiconductor memory

according to claim 1 or 2 characterized by what is controlled to heighten enough the electrical-potential-difference transfer capability of the selection transistor of a non-choosing memory cell and the 1st, and 2 to determine a bit line electrical potential difference with the threshold of the selected memory cell.

[Claim 4] Two or more data circuits which have the function to function as said sense amplifier and to memorize the sensed information as data which control the write-in operating state of a memory cell, The write-in means for performing write-in actuation according to the content of said data circuit corresponding to two or more memory cells in said memory cell array, respectively, The write-in verification means using said threshold detection means in order to check whether the condition after write-in actuation of two or more of said memory cells is in the desired data storage condition, So that it may write in from the content of said data circuit, and the condition after write-in actuation of a memory cell and re-writing may be performed only to the memory cell of imperfection It has the renewal means of the content package of a data circuit which carries out renewal of a package of the content of the data circuit. Said renewal means of the content package of a data circuit The potential of the bit line with which the condition after write-in actuation of a memory cell is outputted is corrected according to the content of the data circuit so that bit line potential may be sensed / memorized as re-write-in data. The data storage condition of a data circuit is held until bit line potential is corrected. A data circuit is operated as a sense amplifier, with the corrected bit line potential held. Perform renewal of a package of the content of the data circuit, and the write-in actuation based on the content of the data circuit, and renewal of the content package of a data circuit The non-volatile semiconductor memory according to claim 2 characterized by what data writing is electrically performed for by carrying out repeating until a memory cell will be in a write-in predetermined condition.

[Claim 5] Said data circuit controls the write-in operating state of a memory cell according to the data memorized in the data circuit at the time of write-in actuation. It controls whether the condition of a memory cell is changed so that it may be in a write-in predetermined condition, or the condition of a memory cell is held in the

condition before write-in actuation. Said renewal means of the content package of a data circuit When the memory cell corresponding to the data circuit where the data which control a memory cell to make it change so that it may be in a write-in predetermined condition are memorized has reached the write-in predetermined condition The data of a data circuit are changed into the data which control the condition of a memory cell to hold in the condition before write-in actuation. When the memory cell corresponding to the data circuit where the data which control a memory cell to make it change so that it may be in a write-in predetermined condition are memorized has not reached a write-in predetermined condition The data which control the condition of a memory cell to make it change so that it may be in a write-in predetermined condition are set as a data circuit. When the data controlled to hold the condition of a memory cell in the condition before write-in actuation in a data circuit are memorized The non-volatile semiconductor memory according to claim 4 characterized by what the data controlled to hold the condition of a memory cell in the condition before write-in actuation are set as a data circuit for.

[Claim 6] In the bit line potential to which the condition after the writing of a memory cell is outputted by said threshold detection means Only the potential of the bit line corresponding to what is data controlled so that the content of said data circuit holds the condition of a memory cell in the condition before write-in actuation It has the bit line potential setting-out circuit set as amendment bit line potential which serves as data controlled to hold the condition of a memory cell in the condition before write-in actuation when it senses in a data circuit. A said renewal of the content package of a data circuit sake, The non-volatile semiconductor memory according to claim 5 characterized by what the potential of the bit line to which the condition after write-in actuation of a memory cell is outputted by the threshold detection means is corrected for by said bit line potential setting-out circuit according to the content of the data circuit.

[Claim 7] Give two or more three or more stored data "i" (i= "0", "1", "2", --, "n-1") to said one memory cell, and multiple-value storage is carried out. The storage condition

corresponding to data "0" is a non-volatile semiconductor memory which is in an elimination condition. Said data circuit The 1st data storage section which memorizes as information whether it controls to hold the condition of a memory cell in the condition before write-in actuation, It is constituted. the 2nd data storage section which memorizes the information which a memory cell should memorize in the case of the information which is not controlled so that the information on the 1st data storage section holds the condition of a memory cell in the condition before write-in actuation, and which writes in and shows data "i" (i= 1, 2, --, n-1) -- since -- Said 1st data storage section was corrected by said bit line potential setting-out circuit according to the content of the data circuit for said renewal of the content package of a data circuit. The non-volatile semiconductor memory according to claim 6 characterized by what it has the function to sense / memorize the potential of the bit line to which the condition after write-in actuation of a memory cell is outputted by the threshold detection means for.

[Claim 8] The 1st data storage section is equipped with the function which senses bit line potential by comparing reference voltage with a bit line electrical potential difference. A said renewal of the content package of a data circuit sake, According to the content of the data circuit, were corrected by said bit line potential setting-out circuit using the reference voltage according to the content of the data circuit. The non-volatile semiconductor memory according to claim 7 characterized by what it has the function to sense / memorize the potential of the bit line to which the condition after write-in actuation of a memory cell is outputted by the threshold detection means for.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to EEPROM which performs the multiple-value storage which makes more information especially to one memory cell than 1 bit memorize with respect to a non-volatile semiconductor memory (EEPROM) rewritable electric.

[0002]

[Description of the Prior Art] The NAND cel mold EEPROM which can be integrated highly is known as one of the EEPROMs. This carries out the series connection of two or more memory cells in the form which shares those sources and a drain by adjoining things, and connects them to a bit line by making this into one unit. A memory cell usually has the FETMOS structure where the laminating of a floating gate (charge accumulation layer) and the control gate was carried out. Accumulation formation of the memory cell array is carried out into p mold well formed in p mold substrate or n mold substrate. The drain side of a NAND cel is connected to a bit line through a selector gate, and a source side is too connected to a common source line through a selector gate. The control gate of a memory cell is continuously arranged in a line writing direction, and serves as a word line.

[0003] This NAND cel type EEPROM of actuation is as follows. Data writing is performed sequentially from the memory cell of the location most distant from the bit line. High tension Vpp (about =20V) is impressed to the control gate of the selected memory cell, intermediate voltage Vppm (about =10V) is impressed to the control gate and the selector gate of a memory cell which are in a bit line side from it, and 0V or intermediate voltage Vm (about =8V) is given to a bit line according to data.

[0004] When 0V are given to a bit line, the potential is transmitted to the drain of a selection memory cell, and electron injection produces it in charge ******. This shifts the threshold of the selected memory cell in the forward direction. This condition is set to "1." When Vm is given to a bit line, electron injection does not happen effectually, therefore a threshold does not change but stops at negative. This condition is set to "0" in the state of elimination. Data writing is simultaneously performed to the memory cell which shares the control gate.

[0005] Data elimination is simultaneously performed to all the memory cells in a NAND cel. That is, all the control gates are set to 0V, and p mold well is set to 20V. At this time, a selector gate, a bit line, and a source line are also set to 20V. Thereby, the electron of a charge accumulation layer is emitted to p mold well by all memory cells, and a threshold is shifted in the negative direction.

[0006] Data read-out sets the control gate of the selected memory cell to 0V, and is performed by detecting whether a current flows by the selection memory cell by making the control gate and the selector gate of the other memory cell into the power-source potential Vcc (for example, 5V).

[0007] The threshold after [constraint of read-out actuation to] "1" writing must be controlled between Vcc(s) from 0V. For this reason, write-in verification is performed, only the memory cell of "1" write-in lack is detected, and re-write-in data are set up so that re-writing may be performed only to the memory cell of "1" write-in lack (it verifies the whole bit). The memory cell of "1" write-in lack is detected by reading by setting the selected control gate to 0.5V (verification electrical potential difference) (verification read-out). That is, if the threshold of a memory cell has a margin to 0V and has not become more than 0.5V, a current will flow by the selection memory cell and it will be detected with "1" write-in lack.

[0008] In the memory cell changed into a "0" write-in condition, since a current naturally flows, the circuit called the verification circuit which compensates the current which flows a memory cell is prepared so that this memory cell may not be taken for "1" writing being insufficient. It writes in a high speed and verification is performed by this

verification circuit.

[0009] Writing in with write-in actuation and repeating verification, to the memory cell of each [carrying out data writing], write-in time amount is optimized and the threshold after "1" writing is controlled between Vcc(s) from 0V.

[0010] It is this NAND cel mold EEPROM, for example, considers setting the condition after writing to three, "0", "1", and "2." For negative and a "1" write-in condition, a threshold is [a "0" write-in condition / a threshold] from 0V. (1/2) A threshold Vcc and a "2" write-in condition (1/2) It carries out to from Vcc to Vcc. In order to judge whether "1" and a "2" write-in condition are reached by whether a verification electrical potential difference is impressed to the control gate, and a current flows by the memory cell in the conventional verification read-out in order that the threshold of a memory cell may judge whether it is more than a verification electrical potential difference, it is 0V about a verification electrical potential difference, respectively. (1/2) It needed to be made Vcc, and needed to check twice and there was a problem that verification read-out took time amount.

[0011]

[Problem(s) to be Solved by the Invention] As mentioned above, when the memory cell tended to be made to memorize multiple-value information in the conventional NAND cel mold EEPROM and it was going to verify the whole bit in the conventional verification circuit, there was a problem that verification read-out took time amount.

[0012] This invention was made in consideration of the above-mentioned situation, the place made into the object can read multiple-value information, without changing a verification read-out electrical potential difference, and it is in offering EEPROM which can aim at compaction of verification read-out time amount.

[0013]

[Means for Solving the Problem] The multiple-value (n value) storage NAND cel mold EEPROM concerning this invention is controlled so that the bit line potential at the time of read-out actuation shows the threshold of a memory cell. This gives 2V to 6V and the selected control gate for example, for a common source line, and makes the potential

of a common source line transmit to a bit line. When bit line potential reaches the threshold of a memory cell, the current which flows a memory cell stops and the bit line potential serves as a value which lengthened the threshold of a memory cell from control gate voltage 2V. If bit line potential is 3V, the threshold of a memory cell is -1V. Non-choosing the control gate and a selector gate are set to 6V so that bit line potential may not be determined with the threshold of a non-choosing memory cell or a selection transistor.

[0014] if an elimination condition is set to "0" and multiple-value level is set to "0", "1", --, "i", --"n-1" at order with the low threshold of a memory cell, in order that verification reading appearance may be carried out and writing may verify a ****** simultaneously about all data "i" enough then, the reference potential when sensing bit line potential according to write-in data is set up. Moreover, if it already writes in and it is detected like [in data "0" writing] that it is enough, the current of a memory cell will be compensated, and if it is detected that it is inadequate in writing, a verification circuit will be prepared so that the current of a memory cell may not be compensated.

[0015] Moreover, it has the 1st register which writes in and memorizes a ****** as data enough, and the 2nd register with which the multiple-value level to write in memorizes "1", --, or of "n-1", and the 1st register also has the function of a sense amplifier to write in and to detect a ****** enough. Furthermore, if there is a memory cell which has not reached a desired write-in condition, it is characterized by having the bit line write-in voltage-output circuit which writes in according to a desired write-in condition, and outputs the bit line electrical potential difference at the time so that re-writing may be performed only to the memory cell.

[0016] Namely, the memory cell array by which the memory cell which enabled electric rewriting which this invention carries out the laminating of a charge accumulation layer and the control gate, is constituted on a semi-conductor layer, and carries out the multiple-value storage of two or more three or more data with a threshold has been arranged in the shape of a matrix, A threshold detection means to charge the bit line connected to a memory cell through this memory cell, and to output the multiple-value

data of a memory cell to a bit line as potential of multiple-value level, a threshold detection means -- the non-volatile semiconductor device equipped with the sense amplifier which senses the bit line potential of the charged multiple-value level is considered as a basic configuration, and it is characterized by the following embodiment.

(1) The every series connection of two or more memory cells is carried out, and they form the NAND cellular structure. The end of a NAND cel is connected to a bit line through the 1st selector gate, and the other end of a NAND cel is connected to a source line through the 2nd selector gate. A threshold detection means A source line electrical potential difference is made to transmit to a bit line through a NAND cel, and a bit line is charged. The selector-gate electrical potential difference of non-choosing control gate voltage and the 1st, and 2 Be controlled to heighten enough the electrical-potential-difference transfer capability of the selection transistor of a non-choosing memory cell and the 1st, and 2 to determine a bit line electrical potential difference with the threshold of the selected memory cell.

(2) Two or more data circuits which have the function to function as a sense amplifier and to memorize the sensed information as data which control the write-in operating state of a memory cell, The write-in means for performing write-in actuation according to the content of the data circuit corresponding to two or more memory cells in a memory cell array, respectively, The write-in verification means using a threshold detection means in order to check whether the condition after write-in actuation of two or more memory cells is in the desired data storage condition, So that it may write in from the content of the data circuit, and the condition after write-in actuation of a memory cell and re-writing may be performed only to the memory cell of imperfection It has the renewal means of the content package of a data circuit which carries out renewal of a package of the content of the data circuit. The renewal means of the content package of a data circuit The potential of the bit line with which the condition after write-in actuation of a memory cell is outputted is corrected according to the content of the data circuit so that bit line potential may be sensed / memorized as re-write-in data. The data storage condition of a data circuit is held until bit line

potential is corrected. A data circuit is operated as a sense amplifier, with the corrected bit line potential held. Perform data writing electrically by performing renewal of a package of the content of the data circuit, and performing write-in actuation based on the content of the data circuit, and renewal of the content package of a data circuit, repeating until a memory cell will be in a write-in predetermined condition.

(3) A data circuit controls the write-in operating state of a memory cell according to the data memorized in the data circuit at the time of write-in actuation. It controls whether the condition of a memory cell is changed so that it may be in a write-in predetermined condition, or the condition of a memory cell is held in the condition before write-in actuation. The renewal means of the content package of a data circuit When the memory cell corresponding to the data circuit where the data which control a memory cell to make it change so that it may be in a write-in predetermined condition are memorized has reached the write-in predetermined condition The data of a data circuit are changed into the data which control the condition of a memory cell to hold in the condition before write-in actuation. When the memory cell corresponding to the data circuit where the data which control a memory cell to make it change so that it may be in a write-in predetermined condition are memorized has not reached a write-in predetermined condition The data which control the condition of a memory cell to make it change so that it may be in a write-in predetermined condition are set as a data circuit. When the data controlled to hold the condition of a memory cell in the condition before write-in actuation in a data circuit are memorized, set the data controlled to hold the condition of a memory cell in the condition before write-in actuation as a data circuit.

(4) In the bit line potential to which the condition after the writing of a memory cell is outputted by the threshold detection means Only the potential of the bit line corresponding to what is data controlled so that the content of the data circuit holds the condition of a memory cell in the condition before write-in actuation It has the bit line potential setting-out circuit set as amendment bit line potential which serves as data controlled to hold the condition of a memory cell in the condition before write-in

actuation when it senses in a data circuit. A renewal of the content package of a data circuit sake, Correct the potential of the bit line to which the condition after write-in actuation of a memory cell is outputted by the threshold detection means by the bit line potential setting-out circuit according to the content of the data circuit.

(5) Give two or more three or more stored data "i" (i= "0", "1", "2", –, "n-1") to one memory cell, and carry out multiple-value storage. The storage condition corresponding to data "0" is a non-volatile semiconductor memory which is in an elimination condition. A data circuit The 1st data storage section which memorizes as information whether it controls to hold the condition of a memory cell in the condition before write-in actuation, It consists of the 2nd data storage section which memorizes the information which a memory cell should memorize in the case of the information which is not controlled so that the information on the 1st data storage section holds the condition of a memory cell in the condition before write-in actuation, and which writes in and shows data "i" (i= 1, 2, ..., n-1). The 1st data storage section should have the function to sense / memorize the potential of the bit line to which the condition after write-in actuation of a memory cell is outputted by the threshold detection means corrected by the bit line potential setting-out circuit according to the content of the data circuit for renewal of the content package of a data circuit.

(6) The 1st data-storage section has the function of sensing / memorizing the potential of the bit line to which the condition after write-in actuation of a memory cell is outputted by the threshold detection means which was equipped with the function which senses bit-line potential, and was corrected by the bit-line potential setting-out circuit according to the content of the data circuit using the reference voltage according to the content of the data circuit for renewal of the content package of a data circuit by comparing reference voltage with a bit-line electrical potential difference.

(7) When it is the information controlled so that the information on the 1st data storage section holds the condition of a memory cell in the condition before write-in actuation, The write-in prevention bit line voltage-output circuit which writes in a bit line and outputs a prevention bit line electrical potential difference at the time of write-in

actuation, In the case of the information which is not controlled so that the information on the 1st data storage section holds the condition of a memory cell in the condition before write-in actuation It had the i-th write-in bit line voltage-output circuit which outputs the bit line electrical potential difference at the time of the i-th writing according to the information which the memory cell of the 2nd data storage section should memorize, and which writes in and shows data "i" (i= 1, 2, --, n-1).

(8) It had a data reversal means for the data of the 1st data storage section which writes in with the data of the 1st data storage section which activates a bit line potential setting-out circuit, and activates a prevention bit line voltage-output circuit to have been reversed, and to reverse the data of the 1st data storage section at the time of write-in actuation before bit line potential setting-out circuit activation.

[0017]

[Function] In this invention, after performing multiple-value data writing, it is detected simultaneously whether the write-in condition of each memory cell has reached the multiple-value level condition of the request. And if there is a memory cell which has not reached desired multiple-value level, it will write in according to a desired write-in condition, and the bit line electrical potential difference at the time will be outputted so that re-writing may be performed only to the memory cell. This write-in actuation and verification read-out are repeated, and data writing will be ended if it checks that all memory cells have reached the desired write-in condition.

[0018] Thus, according to this invention, it can perform at a high speed making small the threshold of the memory cell which data writing ended eventually by repeating write-in actuation gradually, shortening 1 time of write-in time amount, and checking extent of progress of a write-in condition.

[0019]

[Example] Hereafter, the example of this invention is explained with reference to a drawing. Drawing 1 shows the memory cell array 1 of the NAND cel mold EEPROM concerning the 1st example of this invention. The memory cell array 1 is formed on p well or p substrate, and the series connection of the eight memory cells M1-M8 is

carried out between the selection transistor S1 connected to a bit line BL, and the selection transistor S2 connected to the common source line Vs, and it constitutes one NAND cel. Each selection transistor S (S1, S2) has a selector gate SG (SG1, SG2). Each memory cell has the floating gate (charge accumulation layer) and the control gate CG (CG1-CG8) by which laminating formation was carried out, and memorizes information in the amount of the charge stored in a floating gate. The amount of this stored charge can be read as a threshold of a memory cell.

[0020] In this invention, it is shown in drawing 2 , and this threshold is made and read. Here, the memory cell M2 which has the control gate CG 2 is chosen. As shown in drawing 2 (a), an electrical potential difference is impressed to each part, and a bit line BL is made into floating. If the bit line BL is beforehand reset to 0V, a bit line BL will be charged through a NAND cel by the common source line Vs. Each selector gate and control gate voltage are controlled to be decided by the threshold of the memory cell M2 as which the potential of this charged bit line BL was chosen.

[0021] In this example, the control gate CG 2 chosen as 6V in a selector gate 1 and SG 2 and the control gates 3-CG [CG1 and] 8 is set to 2V, and the common source line Vs is set to 6V. The voltage waveform of each part is shown in drawing 2 (b). The threshold not more than 2V can be read by this, and if the threshold of a non-choosing memory cell is controlled less than [2.5V], the threshold beyond -1.5V can be read. If the potential of a bit line BL is 0V and more than 2V and bit line potential of a threshold are 3.5V, a threshold is less than [-1.5V]. If the electrical potential difference of a selector gate 1 and SG 2 and the non-selection-control gates 3-CG [CG1 and] 8 is made sufficiently high, the threshold to -4V can also be read.

[0022] The threshold of the memory cell in this case and the relation of bit line output voltage come to be shown in drawing 3 . Although it will become like a continuous line if it calculates from a threshold in case back bias is 0V, a bit line electrical potential difference serves as back bias actually, and bit line output voltage becomes low like a dashed line. Hereafter, unless it refused for simplification of explanation, an expression called a threshold should take back bias into consideration.

[0023] After an electron is emitted by elimination actuation from the floating gate of a memory cell, an electron is poured into a floating gate by write-in actuation according to write-in data. Drawing 4 reads with write-in time amount in case it reads with the threshold of a non-choosing memory cell and the bit line output voltage at the time is not restricted, and shows the relation of the bit line output voltage at the time. For example, when the electrical potential difference of the common source line at the time of read-out is 3V, unless an electron is poured in to a floating gate and a threshold becomes more than -1V, bit line output voltage does not change. If the threshold of a non-choosing memory cell is a forward value even when the electrical potential difference of a common source line is 6V, the bit line output voltage at the time of read-out will be restricted.

[0024] What is necessary is just to let the condition (threshold about 0-1 V) that data "0" (elimination condition) and bit line output voltage are set to 1-2V in the condition (threshold about -2V- -1 V) that read as shown in drawing 5 , and the bit line output voltage at the time is set to 3-4V be data "1", when you give two conditions (data "0", "1") to one memory cell.

[0025] When giving three conditions (data "0", "1", "2") to one memory cell, The condition (threshold about -2.5V- -1.5 V) that read as shown in drawing 6 , and the bit line output voltage at the time is set to 3.5-4.5V For example, data "0" (elimination condition), What is necessary is just to let the condition (threshold about 1.5 V-2.5V) that data "1" and bit line output voltage are set to 0-0.5V in the condition (it is [about] at a threshold -0.5V-0.5V) that bit line output voltage is set to 1.5-2.5V be data "2."

[0026] Drawing 7 shows the memory cell array 1 of the NOR cel mold EEPROM concerning the 2nd example of this invention. The memory cell array 1 is formed on p well or p substrate, and one memory cell M is arranged between [each] a bit line BL and the common source line Vs. Each memory cell has the floating gate and word line WL by which laminating formation was carried out.

[0027] It is shown in drawing 8 , and the threshold of this memory cell is made and read. As shown in drawing 8 (a), an electrical potential difference is impressed to each

part, and a bit line BL is made into floating. If the bit line BL is beforehand reset to 0V, a bit line BL will be charged through a memory cell by the common source line Vs. The potential of this charged bit line BL is decided by the threshold of the selected memory cell M.

[0028] In this example, a word line WL is set to 6V, and the common source line Vs is set to 6V. The voltage waveform of each part is shown in drawing 8 (b). Thereby, the threshold of 0-6V can be read. If the potential of a bit line BL is 0V and more than 6V and bit line potential of a threshold are 6V, a threshold is less than [0V]. The threshold of the memory cell in this case and the relation of bit line output voltage come to be shown in drawing 9 . Although it will become like a continuous line if it calculates from a threshold in case back bias is 0V, actually, like drawing 3 , a bit line electrical potential difference serves as back bias, and bit line output voltage becomes low like a dashed line.

[0029] After an electron is poured into the floating gate of a memory cell by elimination actuation, an electron is emitted from a floating gate by the write-in actuation according to write-in data. Drawing 10 reads with write-in time amount, and shows the relation of the bit line output voltage at the time. For example, when the electrical potential difference of the common source line at the time of read-out is 3V, if an electron is emitted from a floating gate and a threshold becomes less than [3V], bit line output voltage will not change. Even when the electrical potential difference of a common source line is 6V, it will read, if a threshold becomes less than [0V], and the bit line output voltage at the time will not change.

[0030] What is necessary is just to let the condition (threshold about 2 V-3V) that data "0" (elimination condition) and bit line output voltage are set to 3-4V in the condition (threshold about 4N- 5 V) that read as shown in drawing 11 , and the bit line output voltage at the time is set to 1-2V be data "1", when you give two conditions (data "0", "1") to one memory cell.

[0031] When giving three conditions (data "0", "1", "2") to one memory cell, The condition (V or more [Threshold about 5.5]) that read as shown in drawing 12 , and

the bit line output voltage at the time is set to 0-0.5V For example, data "0" (elimination condition), What is necessary is just to let the condition (threshold about 1.5 V-2.5V) that data "1" and bit line output voltage are set to 3.5-4.5V in the condition (threshold about 3.5 V-4.5V) that bit line output voltage is set to 1.5-2.5V be data "2."

[0032] Drawing 13 shows the configuration of 3 value storage type EEPROM in the 1st and 2nd examples in this invention. The bit line control circuit 2 for controlling the bit line at the time of read-out/writing and the word line actuation circuit 6 for controlling word line potential are formed to the memory cell array 1 ((a), (b)). The bit line control circuit 2 is chosen by the column decoder 3. The bit line control circuit 2 is read with the I / O data conversion circuit 4 through a data input output line (IO line), and exchanges data / write-in data. Since the I / O data conversion circuit 4 outputs outside the multiple-value information on the memory cell by which reading appearance was carried out, it is changed into binary information, and it changes into the multiple-value information on a memory cell the binary information on the write-in data inputted from the outside. The I / O data conversion circuit 4 is connected to the data input output buffer 5 which controls data I/O with the exterior.

[0033] Drawing 14 shows the memory cell array 1 of the NAND cel mold EEPROM in the 1st example, and the concrete configuration of the bit line control circuit 2. The end of a NAND mold cel is connected to a bit line BL, and the other end is connected with the common source line Vs. The memory cell M which a selector gate 1 and SG 2 and the control gates 1-CG 8 are shared by two or more NAND mold cels, and shares the one control gate constitutes a page. A memory cell memorizes data with the threshold Vt, and as shown in said drawing 6 , it memorizes "0", "1", and "2" data. Three conditions are given by one memory cell, and nine kinds of combination is made in two memory cells. Among this, the data for a triplet are memorized by two memory cells using eight kinds of combination.

[0034] In this example, the data for a triplet are memorized in the group of the memory cell of two ****** which share the control gate. Moreover, the memory cell array 1 ((a), (b)) is formed on p well of dedication, respectively.

[0035] A flip-flop 1 and FFs 2 is constituted from the n channel MOS transistors (n-ch Tr.) 8-Qn 10, p channel MOS transistors (p-ch Tr.) 3-Qn 5, n-ch Tr.Qn 11-13, and p-ch Tr.Qn 6-8, respectively, and writing / read-out data is latched. Moreover, it operates also as a sense amplifier. A flip-flop FF 1 writes in "whether do you carry out "0" writing, or carry out "1" or "2" writing", and latches as data information it, and a memory cell reads "whether do you hold the information on "0", or hold the information on "1" or "2"", and latches it as data information. [it] A flip-flop FF 2 writes in "whether do you carry out "1" writing, or carry out "2" writing", and latches as data information it, and a memory cell reads "whether do you hold the information on "2", or hold the information on "0" or "1"", and latches it as data information. [it]

[0036] n-ch Tr.Qn1 will transmit an electrical potential difference Va to a bit line BLa, if precharge signal phipa serves as "H". n-ch Tr.Qn20 will transmit an electrical potential difference Vb to a bit line BLb, if precharge signal phipb serves as "H". n-ch Tr.Qn 4-7 and p-ch Tr.Qp 1-2 transmit electrical potential differences VBHa, VBMa, and VBLa to a bit line BLa selectively according to the data latched to flip-flops FF1 and FF2. n-ch Tr.Qn 14-17 and p-ch Tr.9-10 transmit electrical potential differences VBHb, VBMb, and VBLb to a bit line BLb selectively according to the data latched to flip-flops FF1 and FF2. n-ch Tr.Qn2 connects a bit line BLa with a flip-flop FF 1 because a signal phia1 serves as "H". n-ch Tr.Qn3 connects a bit line BLa with a flip-flop FF 2 because a signal phia2 serves as "H". n-ch Tr.Qn19 connects a bit line BLb with a flip-flop FF 1 because a signal phib1 serves as "H". n-ch Tr.Qn18 connects a bit line BLb with a flip-flop FF 2 because a signal phib2 serves as "H".

[0037] Next, actuation of EEPROM constituted in this way is explained according to drawing 15 -17. In drawing 15 , the timing of read-out actuation and drawing 16 show the timing of write-in actuation, and drawing 17 shows the timing of verification read-out actuation. All have shown the case where control gate CG2a is chosen to the example.

[0038] Read-out actuation is performed by two basic cycles. First, an electrical potential difference Vb is set to 3V, and a dummy bit line and the becoming bit line BLb are

precharged for cycle [1st] read-out. Moreover, precharge signal phipa is set to "L", the subdevice-bit line BLa is made into floating, and the common source line Vsa is set to 6V. Then, selector gates 1a and SG 2a and the control gates 1a, 3a-CG 8a are set to 6V. Control gate CG2a chosen simultaneously is set to 2V. Only when data "0" are written in the selected memory cell, the electrical potential difference of a bit line BLa becomes more than 3V.

[0039] Then, the flip-flop activation signal phin1 and phip1 become "L" and "H", respectively, and a flip-flop FF 1 is reset. A signal phia1 and phib1 become "H", a flip-flop FF 1 and bit lines BLa and BLb are connected, a signal phin1 and phip1 are set to "H" and "L", respectively, bit line potential is sensed, and the information on "whether it is "0" data, "1", or "2" data" is latched to a flip-flop FF 1.

[0040] that cycle [2nd] read-out is read, the 1st cycle and the electrical potential difference of the dummy bit line BLb do not come out 3V, and it is 1V, and Signal phi -- a1 and phi -- b1 and phi -- n1 and phi -- it is different that a signal phia2, phib2, phin2, and phip2 are outputted instead of p1. Therefore, in cycle [2nd] read-out, the information on "whether it is "2" data, "1", or "0" data" is latched to a flip-flop FF 2.

[0041] Reading appearance of the data written in the memory cell is carried out by two read-out cycles explained above. The data of a memory cell are eliminated in advance of data writing, and the threshold Vt of a memory cell has become less than [-1.5V]. Elimination sets p well, the common source line Vsa, and selector gates 1a and SG 2a to 20V, and the control gates 1a-CG 8a are performed as 0V.

[0042] In write-in actuation, precharge signal phipa is first set to "L", and a bit line BLa is made into floating. Vcc and the control gates 1a-CG 8a are set to Vcc for selector-gate SG1a. Selector-gate SG2a writes in and is working 0V. Simultaneously, Signal VRFYa serves as "H" and PBa is served as to "L." Since in "0" writing data are latched so that a node N1 may be set to "L" to a flip-flop FF 1, a bit line BLa is charged by Vcc with an electrical potential difference VBHa. In "1" or "2" writing, a bit line BLa is 0V.

[0043] Then, selector-gate SG1a and the control gates 1a-CG 8a serve as [8V and an electrical potential difference VBMa] 10V and an electrical potential difference VBHa,

and Vrw is served as to 1V. In "1" writing, since data are latched so that a node N3 may be set to "L" to a flip-flop FF 2, 1V are impressed to a bit line BLa with an electrical potential difference VBMa. In "2" writing, in 0V and "0" writing, a bit line BLa is set to 8V. Then, selected control gate CG2a is set to 20V.

[0044] As for the case of "1" or "2" writing, an electron is poured into the charge accumulation layer of a memory cell according to the potential difference of a bit line BLa and control gate CG2a, and the threshold of a memory cell rises. In order to have to lessen the amount of charges which should be poured into the charge accumulation layer of a memory cell as compared with "2" writing, in "1" writing, a bit line BLa is set to 1V, and it is easing the potential difference with control gate CG2a to 19V. At the time of "0" writing, the threshold of a memory cell does not change effectually by bit line electrical-potential-difference 8V.

[0045] At the time of termination of write-in actuation, selector-gate SG1a and the control gates 1a-CG 8a are first set to 0V, and electrical-potential-difference 8V of the bit line BLa at the time of "0" writing are overdue, and are reset by 0V. It is because the data in which the condition of "2" write-in actuation was made temporarily, and it made a mistake at the time of "0" writing will be written if this sequence is reversed.

[0046] In order to check the write-in condition of a memory cell and to perform additional writing only to the memory cell of write-in lack after write-in actuation, verification read-out is performed. Verification read-out resembles cycle [1st] read-out. It is different that reversing the data of a flip-flop FF 1 first, an electrical potential difference's Vb serving as Vcc, and Signals VRFYa and VRFYb are outputted, and electrical potential differences VBLb and VBMb are then set to 2.5V and 0.5V, respectively. The electrical potential difference of the dummy bit line BLb is determined by the data of an electrical potential difference Vb, VBLb, VBMb, and a flip-flop 1 and FFs 2. after, as for Signals VRFYa and VRFYb, selector gates 1a and SG 2a and the control gates 1a-CG 8a were reset by 0V -- a signal phin1 and phip1 -- respectively -- "L" and "H" -- it is outputted in front. In other words, after determining the potential of a bit line BLa by the threshold of a memory cell, before a flip-flop FF 1 is reset, it is.

[0047] Reversal actuation is explained for the data of a flip-flop FF 1. First, an electrical potential difference Vb is set to 2.5V, and a dummy bit line and the becoming bit line BLb are precharged. Moreover, precharge signal phipa and phipb are set to "L", and bit lines BLa and BLb are made into floating. Then, Signal PBa is set to "L", and only when a node N1 is "L", a bit line BLa is charged more than 2.5V. Then, the flip-flop activation signal phin1 and phip1 become "L" and "H", respectively, and a flip-flop FF 1 is reset. A signal phia1 and phib1 become "H", a flip-flop FF 1 and bit lines BLa and BLb are connected, a signal phin1 and phip1 are set to "H" and "L", respectively, and bit line potential is sensed. The data of a flip-flop FF 1 are reversed by this actuation.

[0048] Next, the electrical potential difference of the bit line BL after the data reversal actuation decided by the threshold of the data (data1) latched to the flip-flop FF 1, the data (data2) latched to the flip-flop FF 2, and the selected memory cell is explained. data1 controls "whether it is writing, "1", or "0" "2" writing", and, in "0" writing, in H", "1", or ""2" writing, a node N1 is [a node N1] "L" after data reversal actuation after data reversal actuation. data2 controls "whether they are writing and "1" "2" writing", and, in "1" writing, in "L" and "2" writing, a node N3 is [a node N3] "H".

[0049] In the verification read-out actuation after "0" data writing, it is not based on the condition of a memory cell, but a bit line BL becomes "L" with the electrical potential differences VBLa and VBMa of 0V because Signal VRFYa serves as "H". Therefore, a bit line BLa is sensed and the re-write-in data latched are "0" so that a node N1 may be set to "L" with a flip-flop FF 1.

[0050] In the verification read-out actuation after "1" data writing, Signal VRFYb serves as "H" and the dummy bit line BLb is set to 2.5V. Therefore, when the memory cell has not reached a "1" write-in condition, a bit line BLa is more than 2.5V, a bit line BLa is sensed and the re-write-in data latched are "1" so that a node N1 may become "H" with a flip-flop FF 1. When the memory cell has reached the "1" write-in condition, a bit line BLa is less than [2.5V], a bit line BLa is sensed and the re-write-in data latched are "0" so that a node N1 may be set to "L" with a flip-flop FF 1.

[0051] In the verification read-out actuation after "2" data writing, Signal VRFYb serves

as "H" and the dummy bit line BLb is set to 0.5V. Therefore, when the memory cell has not reached a "2" write-in condition, a bit line BLa is more than 0.5V, a bit line BLa is sensed and the re-write-in data latched are "2" so that a node N1 may become "H" with a flip-flop FF 1. When the memory cell has reached the "2" write-in condition, a bit line BLa is less than [0.5V], a bit line BLa is sensed and the re-write-in data latched are "0" so that a node N1 may be set to "L" with a flip-flop FF 1. By this verification read-out actuation, from the write-in condition of write-in data and a memory cell, re-write-in data are set up, as shown in the following (table 1).

[0052]

[A table 1]

書き込みデータ	0	0	0	1	1	2	2	2
メモリセルのデータ	0	1	2	0	1	0	1	2
再書き込みデータ	0	0	0	1	0	2	2	0

this (table 1) -- from -- it should be in a "1" write-in condition as [understand] -- nevertheless -- the memory cell of "1" write-in lack -- again -- "1" -- writing is performed and it should be in a "2" write-in condition -- nevertheless -- "2" -- "2" writing is again performed only to the memory cell of write-in lack.

[0053] Data writing is performed by repeating write-in actuation and verification read-out actuation, and performing them. The potential of each part of a memory cell array at the time of elimination, writing, read-out, and verification read-out is shown in the following (table 2).

[0054]

[A table 2]

	消去	書き込み "0" "1" "2"	読み出し 第1ページ	第2ページ	ベリファイ 読み出し
BLa	20V	8V 1V 0V	"0"書き込み後 "H"	"2"書き込み後 "L"	図17参照
SG1a	20V	10V	6V	6V	6V
CG1a	0V	10V	6V	6V	6V
CG2a	0V	20V	2V	2V	2V
CG3a	0V	10V	6V	6V	6V
CG4a	0V	10V	6V	6V	6V
CG5a	0V	10V	6V	6V	6V
CG6a	0V	10V	6V	6V	6V
CG7a	0V	10V	6V	6V	6V
CG8a	0V	10V	6V	6V	6V
SG2a	20V	0V	6V	6V	6V
Vsa	20V	0V	6V	6V	6V
pウェル	20V	0V	0V	0V	0V

[0055] Drawing 18 shows the memory cell array 1 of the NOR cel mold EEPROM in the 2nd example, and the concrete configuration of the bit line control circuit 2. The end of a NOR mold cel is connected to a bit line BL, and the other end is connected with the common source line Vs. The memory cell M which a word line WL is shared by two or more NOR mold cels, and shares one word line constitutes a page. A memory cell memorizes data with the threshold Vt, and memorizes "0", "1", and "2" data like drawing 12 . Three conditions are given by one memory cell, and nine kinds of combination is made in two memory cells. Among this, the data for a triplet are memorized by two memory cells using eight kinds of combination. In this example, the data for a triplet are memorized in the group of the memory cell of two ****** which share a word line. Moreover, the memory cell array 1 ((a), (b)) is formed on p substrate.

[0056] A flip-flop 3 and FFs 4 is constituted from n-ch Tr.Qn 26-28, p-ch Tr.Qn 15-17 and n-ch Tr.Qn 29-31, and p-ch Tr.Qn 18-20, respectively, and writing / read-out data is latched. Moreover, it operates also as a sense amplifier. A flip-flop FF 3 writes in "whether do you carry out "0" writing, or carry out "1" or "2" writing", and latches as data information it, and a memory cell reads "whether do you hold the information on "0", or hold the information on "1" or "2"", and latches it as data information. [it] A flip-flop FF 4 writes in "whether do you carry out "1" writing, or carry out "2" writing",

and latches as data information it, and a memory cell reads "whether do you hold the information on "2", or hold the information on "0" or "1"", and latches it as data information. [it]

[0057] n-ch Tr.Qn21 will transmit an electrical potential difference Va to a bit line BLa, if precharge signal phipa serves as "H". n-ch Tr.Qn36 will transmit an electrical potential difference Vb to a bit line BLb, if precharge signal phipb serves as "H". n-ch Tr.Qn 24 and 25 and p-ch Tr.11-14 transmit selectively electrical potential differences VBHa and VBMa and 0V to a bit line BLa according to the data latched to flip-flops FF3 and FF4. n-ch Tr.Qn 32 and 33 and p-ch Tr.21-24 transmit selectively electrical potential differences VBHb and VBMb and 0V to a bit line BLb according to the data latched to flip-flops FF3 and FF4. n-ch Tr.Qn22 connects a bit line BLa with a flip-flop FF 3 because a signal phia1 serves as "H". n-ch Tr.Qn23 connects a bit line BLa with a flip-flop FF 4 because a signal phia2 serves as "H". n-ch Tr.Qn35 connects a bit line BLb with a flip-flop FF 3 because a signal phib1 serves as "H". n-ch Tr.Qn34 connects a bit line BLb with a flip-flop FF 4 because a signal phib2 serves as "H".

[0058] Next, actuation of EEPROM constituted in this way is explained according to drawing 19 -21. In drawing 19 , the timing of read-out actuation and drawing 20 show the timing of write-in actuation, and drawing 21 shows the timing of verification read-out actuation. All have shown the case where a word line WLa is chosen to the example.

[0059] Read-out actuation is performed by two basic cycles. First, an electrical potential difference Vb is set to 1V, and a dummy bit line and the becoming bit line BLb are precharged for cycle [1st] read-out. Moreover, precharge signal phipa is set to "L", the subdevice-bit line BLa is made into floating, and the common source line Vsa is set to 6V. Then, a word line WLa is set to 6V. Only when data "0" are written in the selected memory cell, the electrical potential difference of a bit line BLa becomes less than [0.5V].

[0060] Then, the flip-flop activation signal phin1 and phip1 become "L" and "H", respectively, and a flip-flop FF 3 is reset. A signal phia1 and phib1 become "H", a

flip-flop FF 3 and bit lines BLa and BLb are connected, a signal phin1 and phip1 are set to "H" and "L", respectively, bit line potential is sensed, and the information on "whether it is "0" data, "1", or "2" data" is latched to a flip-flop FF 3.

[0061] that cycle [2nd] read-out is read, the 1st cycle and the electrical potential difference of the dummy bit line BLb do not come out 1V, and it is 3V, and Signal phi -- a1 and phi -- b1 and phi -- n1 and phi -- it is different that a signal phia2, phib2, phin2, and phip2 are outputted instead of p1. Therefore, in cycle [2nd] read-out, the information on "whether it is "2" data, "1", or "0" data" is latched to a flip-flop FF 4.

[0062] Reading appearance of the data written in the memory cell is carried out by two read-out cycles explained above. The data of a memory cell are eliminated in advance of data writing, and the threshold Vt of a memory cell has become more than 5.5V. A word line WLa is set to 20V, and a bit line BLa is performed as 0V.

[0063] In write-in actuation, precharge signal phipa is first set to "L", and a bit line BLa is made into floating. Then, Signal VRFYBa is served as to "L" and Pa serves as "H". Since in "0" writing data are latched so that a node N5 may become "H" to a flip-flop FF 3, a bit line BLa is set to 0V. In "1" or "2" writing, a bit line BLa is set to Vcc by electrical potential differences VBHa and VBMa.

[0064] Then, 8V and an electrical potential difference VBMa are set to 7V by electrical potential differences VBHa and Vrw. In "1" writing, since data are latched so that a node N7 may become "H" to a flip-flop FF 4, 7V are impressed to a bit line BLa with an electrical potential difference VBMa. In "2" writing, in 8V and "0" writing, a bit line BLa is set to 0V. Then, the selected word line WLa is set to -12V.

[0065] In "1" or "2" writing, an electron is emitted by the potential difference of a bit line BLa and a word line WLa from the charge accumulation layer of a memory cell, and the threshold of a memory cell falls. In order to have to lessen the amount of charges which should be emitted from the charge accumulation layer of a memory cell as compared with "2" writing, in "1" writing, a bit line BLa is set to 7V, and it is easing the potential difference with a word line WLa to 19V. At the time of "0" writing, the threshold of a memory cell does not change effectually by bit line

electrical-potential-difference 0V.

[0066] In order to check the write-in condition of a memory cell and to perform additional writing only to the memory cell of write-in lack after write-in actuation, verification read-out is performed. Verification read-out resembles cycle [1st] read-out. It is different that reversing the data of a flip-flop FF 3 first, an electrical potential difference's Vb being 0V, and Signals VRFYBa and VRFYBb are outputted, and electrical potential differences VBHb and VBMb are then set to 1.5V and 3.5V, respectively. The electrical potential difference of the dummy bit line BLb is determined by the data of an electrical potential difference Vb, VBHb, VBMb, and a flip-flop 3 and FFs 4. after, as for Signals VRFYBa and VRFYBb, the word line WLa was reset by 0V -- a signal phin1 and phip1 -- respectively -- "L" and "H" -- it is outputted in front. In other words, after determining the potential of a bit line BLa by the threshold of a memory cell, before a flip-flop FF 3 is reset, it is.

[0067] First, reversal actuation is explained for the data of a flip-flop FF 1. Electrical potential differences Va and Vb are first set to Vcc and 2.5V, respectively, and bit lines BLa and BLb are precharged. Moreover, precharge signal phipa and phipb are set to "L", and bit lines BLa and BLb are made into floating. Then, Signal Pa serves as "H", and only when a node N3 is "H", a bit line BLa discharges less than [2.5V]. Then, the flip-flop activation signal phin1 and phip1 become "L" and "H", respectively, and a flip-flop FF 3 is reset. A signal phia1 and phib1 become "H", a flip-flop FF 3 and bit lines BLa and BLb are connected, a signal phin1 and phip1 are set to "H" and "L", respectively, and bit line potential is sensed. The data of a flip-flop FF 3 are reversed by this actuation.

[0068] Next, the electrical potential difference of the bit line BL after the data reversal actuation decided by the threshold of the data (data1) latched to the flip-flop FF 3, the data (data2) latched to the flip-flop FF 4, and the selected memory cell is explained. data1 "is writing, "1", or "0" "2" writing" -- controlling -- the case of "0" writing -- a node N5 -- after data reversal actuation -- the case of "L", "1", or "2" writing -- a node N5 -- after data reversal actuation -- "H" -- it is. data2 controls "whether they are

writing and "1" "2" writing", and, in "1" writing, in H" and ""2" writing, a node N7 is [a node N7] "L."

[0069] In the verification read-out actuation after "0" data writing, it is not based on the condition of a memory cell, but a bit line BLa serves as "H" with electrical potential differences VBHa and VBMa by Signal VRFYBa being set to "L." Therefore, a bit line BLa is sensed and the re-write-in data latched are "0" so that a node N5 may become "H" with a flip-flop FF 3.

[0070] In the verification read-out actuation after "1" data writing, Signal VRFYBb is set to "L" and the dummy bit line BLb is set to 1.5V. Therefore, when the memory cell has not reached a "1" write-in condition, a bit line BLa is less than [1.5V], a bit line BLa is sensed and the re-write-in data latched are "1" so that a node N5 may be set to "L" with a flip-flop FF 3. When the memory cell has reached the "1" write-in condition, a bit line BLa is more than 1.5V, a bit line BLa is sensed and the re-write-in data latched are "0" so that a node N5 may become "H" with a flip-flop FF 3.

[0071] In the verification read-out actuation after "2" data writing, Signal VRFYBb is set to "L" and the dummy bit line BLb is set to 3.5V. Therefore, when the memory cell has not reached a "2" write-in condition, a bit line BLa is less than [3.5V], a bit line BLa is sensed and the re-write-in data latched are "2" so that a node N5 may be set to "L" with a flip-flop FF 3. When the memory cell has reached the "2" write-in condition, a bit line BLa is more than 3.5V, a bit line BLa is sensed and the re-write-in data latched are "0" so that a node N5 may become "H" with a flip-flop FF 3.

[0072] By this verification read-out actuation, re-write-in data are set up like the above (table 1) from the write-in condition of write-in data and a memory cell. it should be in a "1" write-in condition as [show / (a table 1)] -- nevertheless -- the memory cell of "1" write-in lack -- again -- "1" -- writing is performed and it should be in a "2" write-in condition -- nevertheless -- "2" -- "2" writing is again performed only to the memory cell of write-in lack.

[0073] Data writing is performed by repeating write-in actuation and verification read-out actuation, and performing them. The potential of each part of a memory cell array at

the time of elimination, writing, read-out, and verification read-out is shown in the following (table 3).

[0074]

[A table 3]

	消去	書き込み			読み出し		ベリファイ
		"0"	"1"	"2"	第1サイクル	第2サイクル	読み出し
BLa	0V	0V	7V	8V	"0"書き込み時のみ "L"	"2"書き込み時のみ "H"	図21参照
WLa	20V	-12V			6V	6V	6V
Vsa	0V	0V			6V	6V	6V

[0075] Drawing 22 is a circuit which controls the data I/O between the I / O data conversion circuits 4 looked at by the flip-flop 3 and FFs 4 looked at by the flip-flop 1 and FFs 2 looked at by drawing 14 or drawing 18 and drawing 13 . If the column decoder 3 is constituted from an inverter I1 and NAND circuit G1 and the column activation signal CENB serves as "H", the decoder output chosen by the address signal will serve as "H", and Nodes A, B, C, and D will be connected with IOA1, IOB1, IOA2, and IOB2, respectively. Nodes A, B, C, and D are nodes 6, 5, 8, and N 7 in a node 1, 2, 3, and N 4 and drawing 18 at drawing 14 , respectively. Read-out / write-in data when a bit line BLa is chosen, and the relation of IOA1, IOB1, IOA2, and IOB2 are as in the following (table 4).

[0076]

[A table 4]

書き込みデータ	IOA1	IOB1	IOA2	IOB2
0	L	H	—	—
1	H	L	L	H
2	H	L	H	L

(a)

読み込みデータ	IOA1	IOB1	IOA2	IOB2
0	H	L	H	L
1	L	H	H	L
2	L	H	L	H

(b)

[0077]

[Effect of the Invention] Controlling buildup of circuit area according to this invention, as explained above Three write-in conditions are set [in addition] as one memory cell. And and write-in time amount until it changes into each write-in condition of each memory cell By performing write-in verification control, it can optimize independently and EEPROM which made it possible to store threshold distribution of the memory cell written in eventually in the range small at a high speed can be obtained. Moreover, also when setting two or four write-in conditions or more as one memory cell, it is possible if the main point of this invention is followed.